UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/799,852	03/12/2004	Isamu Miyanishi	2271/71532	2074

7590 08/28/2007

Ivan S. Kavrukov, Esq.
Cooper & Dunham LLP
1185 Avenue of the Americas
New York, NY 10036

EXAMINER	
ZAMAN, FAISAL M	

ART UNIT	PAPER NUMBER
2111	

MAIL DATE	DELIVERY MODE
08/28/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/799,852	MIYANISHI ET AL.	
	Examiner	Art Unit	
	Faisal Zaman	2111	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 August 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *12 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. **Claims 1 and 10** are rejected under 35 U.S.C. 102(b) as being anticipated by Kasebayashi et al. ("Kasebayashi") (U.S. Patent No. 5,758,191).

Regarding Claims 1 and 10, Kasebayashi discloses a communications interface apparatus (Figure 2, item 100, Column 4, lines 57-61) comprising:

A register circuit storing data to be transferred to a host computer (Figure 3, item 11, Column 5, lines 46-49);

A first memory storing first information indicating a specific address of the register circuit and representing an access to the communications interface apparatus executed by the host computer for a data transfer (Figure 3, item 12, Column 5, lines 49-52);

A second memory storing second information, sent in association with the first information stored in the first memory and corresponding to said data to be transferred to said host computer, to be written into the register circuit at the specific address indicated by the first information stored in the first memory (Figure 3, item 14, Column 5, lines 57-61; ie. the read unit 14 actively reading data from magnetic disk 13 and

separately writing the data to buffer 11 [using two distinct steps] would indicate that internal memory is necessarily required); and

A control circuit configured to perform an information writing operation for writing the first information into the first memory and the second information into the second memory in chronological order of accesses executed, in connection with said data to be transferred to said host computer (Figure 3, item 14, Column 5, lines 57-61; it is understood that the read unit 14 comprises of both a memory and a control circuit since both functions are performed as disclosed in Kasebayashi).

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. **Claims 2, 3, 9, 11, 12, 18, and 21** are rejected under 35 U.S.C. 103(a) as being unpatentable over Kasebayashi in view of Tsuda et al. ("Tsuda") (U.S. Patent No. 6,799,242).

Kasebayashi discloses the communications interface apparatus according to Claim 1 as described above.

Regarding Claim 2, 3, 11, and 12, Kasebayashi discloses wherein the control circuit performs the information writing and reading operation for writing and reading the

first information into the first memory and the second information into the second memory in chronological order of accesses executed (Kasebayashi, Figure 3, item 17, Column 6, lines 5-10).

Kasebayashi does not expressly disclose wherein the control circuit performs the information writing operation for writing the first information into the first memory and the second information into the second memory in chronological order of accesses executed, when an operation mode of the communications interface apparatus is changed from a low power consumption mode to a regular operation mode.

In the same field of endeavor (e.g. reading data from a disc for use by a computer), Tsuda discloses wherein a control circuit performs an information writing operation to write a first information into a first memory (Tsuda, Column 8, lines 19-21; ie. TOC transfer command being transferred to memory control circuit 61) and a second information into a second memory in chronological order of accesses executed (Tsuda, Column 8, lines 21-25; ie. TOC data is transferred from SRAM 56 to buffer RAM 7), when an operation mode of the communications interface apparatus is changed from a low power consumption mode to a regular operation mode (Column 8, lines 11-12; ie. sleep mode to normal operational mode).

Accordingly, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have combined Tsuda's teachings of reading data from a disc for use by a computer to the teachings of Kasebayashi, for the purpose of providing a disc apparatus having a reduced power consumption during a sleep mode for greater efficiency in a computing system (see Tsuda, Column 3, lines 28-30).

Kasebayashi also provides motivation to combine by stating it is an object of the invention to increase efficiency in a disc apparatus that communicates with a host system (see Kasebayashi, Column 2, lines 18-23).

Regarding Claims 9 and 18, the examiner takes Official Notice that the integration of a register circuit, a first and second memory, and a control circuit into a single integrated chip in the type of system disclosed was well-known in the art at the time of the Applicant's invention and the use of it would not change the scope of the invention. Therefore, it would be obvious to one of ordinary skill in the art to integrate the register circuit, the first and second memories, and the control circuit into a single integrated chip.

Regarding Claim 21, Tsuda teaches wherein a communications interface apparatus (Tsuda, Figure 7) is configured to enable data transmission from an optical disk drive device (Tsuda, Figure 1, item 2) to a host computer (Tsuda, Figure 1, Column 1, lines 43-47).

The motivation that was used in the combination of Claim 2, super, applies equally as well to Claim 21.

5. **Claims 4-6 and 13-15** are rejected under 35 U.S.C. 103(a) as being unpatentable over Kasebayashi in view of Tsuda as applied to Claim 2 above

(hereinafter "Kasebayashi-Tsuda"), and further in view of Yamada et al. ("Yamada") (U.S. Patent No. 6,470,439).

Kasebayashi-Tsuda discloses the invention substantially as claimed.

Regarding Claims 4 and 13, Kasebayashi-Tsuda discloses wherein the control circuit conducts the information writing operations with respect to the first and second memories (Kasebayashi, Figure 3, item 12 and item 17, respectively) in synchronism with each other and conducts the information reading operations with respect to the first and second memories in synchronism with each other (Kasebayashi, Column 6, lines 1-5).

In same field of endeavor (e.g. the use of a memory control circuit in controlling memory used in various electronic devices), Yamada teaches the following limitation, which Kasebayashi-Tsuda does not expressly disclose:

Wherein a memory comprises a first-in and first-out memory (Yamada, title, abstract) including a specific number of buffer areas into which data from an external device is written (Yamada, Column 3, lines 18-31).

Accordingly, it would have been obvious to one of ordinary skill in the art at the time of the invention was made to have incorporated Yamada's teachings of the use of a memory control circuit in controlling memory used in various electronic devices with the teachings of Kasebayashi-Tsuda, for the purpose of providing a FIFO memory control circuit in which the amount of effective data in a memory can be correctly counted so that when the frequencies of a read clock and a write clock are different, data is prevented from being lost by being overwritten, and data is prevented from being

read out twice (see Yamada, Column 6, lines 18-22). Kasebayashi-Tsuda provides motivation to combine by stating it is an object of the present invention to have an efficient system while reducing power consumption in a device during a sleep mode (see Tsuda, Column 3, lines 28-30).

Regarding Claims 5 and 14, Yamada discloses the following, which Kasebayashi-Tsuda does not expressly disclose:

Wherein the control circuit accesses the first and second memories in synchronism with a first clock signal for the information writing operation and a second clock signal for the information reading operation (Yamada, Column 3, lines 26-31), and wherein a first frequency of the first clock signal is greater than a second frequency of the second clock signal (Yamada, Column 4, lines 43-52).

The motivation that was utilized in the combination of Claim 4, super, applies equally as well to Claim 5.

Regarding Claims 6 and 15, Kasebayashi-Tsuda discloses wherein the control circuit performs the information writing and reading operation for writing and reading the first information into the first memory and the second information into the second memory in chronological order of accesses executed (Kasebayashi, Figure 3, item 17, Column 6, lines 5-10) when an operation mode of the communications interface apparatus is changed from a low power consumption mode to a regular operation mode (Tsuda, Column 8, lines 11-12; ie. sleep mode to normal operational mode).

Kasebayashi-Tsuda does not expressly disclose wherein the information writing and reading operation is performed without buffering the first and second information in the first-in and first-out memories in an event that the respective first-in and first-out memories of the first and second memories are in a memory empty state after the first and second information stored in the respective first-in and first-out memories of the first and second memories, respectively, are transferred to the register circuit when the operation mode of the communications interface apparatus is changed from a low power consumption mode to a regular operation mode.

In the same field of endeavor, Yamada teaches wherein data is not written (ie. is not buffered) into a FIFO memory in the event that a FULL signal is sent from the memory control circuit, indicating the FIFO memory is full (Yamada, Column 4, lines 12-22).

The motivation that was utilized in the combination of Claim 4, super, applies equally as well to Claim 6.

6. **Claims 7-8 and 16-17** are rejected under 35 U.S.C. 103(a) as being unpatentable over Kasebayashi in view of Tsuda and Yamada as applied to Claim 4 above (hereinafter, "KTY"), and further in view of Chuang et al. ("Chuang") (U.S. Patent No. 6,502,159).

KTY discloses the communications interface apparatus according to Claim 6, as described above.

Regarding Claims 7 and 16, KTY does not expressly disclose wherein each of the first and second memories comprises a selection circuit configured to select one of (i) a first data path for the first and second information not via the first and second memories and (ii) a second data path for the first and second information via the respective first and second memories, on an exclusive basis according to a control signal from the control circuit and to output corresponding data to the register circuit through the selected one of the first and second data paths.

In the same field of endeavor (e.g. data transfers between a disk drive apparatus and a host computer), Chuang teaches wherein a circuit (Chuang, Figure 2, item 105, Column 4, lines 22-23) comprises a selection circuit (Chuang, Figure 3, item 120, Column 4, lines 36-50) configured to select one of (i) a first data path for information not via a memory (Chuang, Table 2, Column 4, lines 26-29) and (ii) a second data path for the information via a memory (Chuang, Table 1, Column 4, lines 23-25), on an exclusive basis according to a control signal from a control circuit (Chuang, Figure 2, item 12, Column 3, lines 56-60) and to output corresponding data to a circuit (Chuang, Figure 3, item 57, Column 3, lines 56-60) through the selected one of the first and second data paths.

Accordingly, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have combined Chuang's teachings of data transfers between a disk drive apparatus and a host computer with the teachings of KTY, for the purpose of greatly reducing system memory usage and bus utilization (see Chuang, Column 3, lines 52-55) and to reduce unnecessary data flow in the system and

unnecessary consumption of system resources (see Chuang, Column 3, lines 60-64). KTY also provides motivation to combine by stating it is an object of the invention to increase efficiency in a disc apparatus that communicates with a host system (see Kasebayashi, Column 2, lines 18-23).

Regarding Claims 8 and 17, KTY discloses wherein the control circuit comprises:

A data writing circuit block configured to write the first and second information into the first and second memories, respectively, in accordance with an access performed by the host computer (Kasebayashi, Figure 3, item 17, Column 6, lines 5-10);

A data reading circuit block configured to start reading the first and second information from the first and second memories, respectively, upon a time the write control circuit block starts writing the first and second information into the first and second memories, respectively (Kasebayashi, Figure 3, item 17, Column 6, lines 5-10);

A status detecting circuit block configured to detect memory statuses of the first-in and first-out memories included in the respective first and second memories and to output a status signal representing the memory statuses detected (Yamada, Column 4, lines 12-22; see combination of Claim 6 above); and

A selection control circuit block configured to control accesses to the respective first and second memories in accordance with a status as to whether the operation mode of the communications interface apparatus is the low power consumption mode

and the status signal output from the status detecting circuit block (Yamada, Column 4, lines 12-22 and Tsuda, Column 8, lines 11-12; see combination of Claim 6 above).

KTY does not expressly disclose wherein the selection control circuit block is configured to control the selection circuits included in the respective first and second memories.

In the same field of endeavor, Chuang teaches wherein a selection control circuit block (Chuang, Figure 2, item 105, Column 4, lines 22-23) is configured to control the selection circuit (Chuang, Figure 3, item 120, Column 4, lines 36-50) included in a circuit in accordance with a status from a control circuit (Chuang, Figure 2, item 12, Column 3, lines 56-60).

The motivation used in the combination of Claim 7, super, applies equally as well to Claim 8.

7. **Claims 19 and 20** are rejected under 35 U.S.C. 103(a) as being unpatentable over Kasebayashi, Tsuda, and Silvester (U.S. Patent No. 6,631,469).

Regarding Claim 19, Kasebayashi teaches a disk drive apparatus (Kasebayashi, Figure 2, item 100), comprising:

An interface circuit for interfacing communications, between a disk drive mechanism and a host computer (Kasebayashi, Figure 2, item 105, Column 4, lines 64-66), the interfacing circuit comprising:

An input terminal for receiving data sent from the host computer (Kasebayashi, Figure 2, see connection between items 200 and 105, Column 4, lines 64-66);

A data processor configured to perform a predetermined data processing operation to the data received through the input terminal (Kasebayashi, Figure 2, item 101, Column 4, lines 62-64); and

A buffering circuit block configured to buffer the data received through the input terminal (Kasebayashi, Figure 3, Column 5 line 36 – Column 6 line 13).

Kasebayashi does not expressly teach wherein the disk drive apparatus is an optical disk drive apparatus;

An optical disk drive mechanism;

A clock generator configured to generate a clock signal with which the data processor performs the predetermined data processing operation; and

An operation mode changer configured to control the clock generator to reduce a frequency of the clock signal to a value smaller than a predetermined value to change an operation mode from a regular operation mode to a low power consumption mode; and

Wherein the buffering circuit block includes:

A first data transfer path configured to transfer the data received through the input terminal to the data processor not via a memory, and

A second data transfer path configured to transfer the data received through the input terminal to the data processor via a memory; and

A path selection controller configured to control the buffering circuit block to select the second data transfer path on an exclusive basis when the operation mode is changed from the regular operation mode to the low power consumption mode.

In the same field of endeavor (e.g. reading data from a disc for use by a computer), Tsuda teaches an optical disk drive mechanism (Tsuda, Figure 1, Column 1, lines 19-23);

A clock generator configured to generate a clock signal with which the data processor performs the predetermined data processing operation (Tsuda, Figure 7, item 62, Column 8, lines 11-25); and

An operation mode changer configured to control the clock generator to reduce a frequency of the clock signal to a value smaller than a predetermined value to change an operation mode from a regular operation mode to a low power consumption mode (Tsuda, Column 7 line 56 – Column 8 line 10).

Accordingly, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have combined Tsuda's teachings of reading data from a disc for use by a computer to the teachings of Kasebayashi, for the purpose of providing a disc apparatus having a reduced power consumption during a sleep mode for greater efficiency in a computing system (see Tsuda, Column 3, lines 28-30).

Also in the same field of endeavor (e.g. transfer of data between an I/O device and a processor using a low power mode), Silvester teaches wherein a circuit block includes:

A first data transfer path configured to transfer the data received through an input terminal to a data processor not via a memory (Silvester, Figure 1, see data transfer path between items 100 and 120/125/130), and

A second data transfer path configured to transfer the data received through the input terminal to the data processor via a memory (Silvester, Figure 1, item 116, Column 4, lines 39-47; ie. low power non-volatile memory 116 is only used for data destined for processor 100 from devices 120/125/130 in a low power mode); and

A path selection controller configured to control the buffering circuit block to select the second data transfer path on an exclusive basis when the operation mode is changed from the regular operation mode to the low power consumption mode (Silvester, Figure 1, item 116, Column 4, lines 39-47).

Accordingly, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have combined Silvester's teachings of transfer of data between an I/O device and a processor using a low power mode with the teachings of Kasebayashi, for the purpose of continually storing and updating a computer system, but with using very little battery power (see Silvester, Column 2, lines 9-15).

Regarding Claim 20, Silvester teaches wherein the path selection controller selects one of the first and second data transfer paths for a write operation (Silvester, Column 4, lines 42-43).

The motivation that was used in the combination of Claim 19, super, applies equally as well to Claim 20.

Response to Arguments

8. Applicant's arguments filed 8/20/2007 have been fully considered but they are not persuasive.

Regarding Claims 1 and 10, Applicant argues that "the read unit 14 in the system proposed by Kasebayashi, contrary to the contention in the Office Action, does not store data from the magnetic disk 13", and further "[i]t can be seen clearly in Fig. 3 of Kasebayashi that the data from the magnetic disk 13 flows directly to the buffer 11." The examiner respectfully disagrees. Contrary to Applicant's argument, Kasebayashi does in fact teach this limitation. In Column 5, lines 57-61 of Kasebayashi, it is stated that "read unit 14 ... reads data required by the host system 10 from the magnetic disk 13, and writes the data in the read/write area indicated by the address information." The term "read", as defined by the Microsoft Computer Dictionary, Fifth Edition (attached), is "[t]he action of transferring data from an input source into a computer's memory" (see definition [1]). Therefore, it can be seen that read unit 14 does in fact store data from the magnetic disk 13.

Also with regards to Claims 1 and 10, Applicant argues that "the address storage unit 12 of Kasebayashi does not correspond to the data to be transferred to the host computer", and further "the address storage unit 12 of Kasebayashi does not store specific addresses corresponding to the data to be transferred to the host computer". However, the claim language recites the "first memory [i.e., the address storage unit 12] stor[es] first information indicating a specific address of the register circuit ...". The buffer area 11 was equated to the claimed "register circuit" in the rejection. Therefore,

as described in Column 5, lines 49-52 and Column 6, lines 14-54 of Kasebayashi, the address storage unit 12 does in fact store "first information indicating a specific address of the register circuit (i.e., buffer area 11)". In response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., the address storage unit 12 storing specific addresses corresponding to the data to be transferred to the host computer) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

Regarding Claim 19, Applicant argues that "the clock generator 62 is not configured to supply the clock signals at all to the host interface 13 ... or other parts of data processing circuit 260", and further "the interface 13 remains active while the remainder of the optical disk player enters the sleep mode." However, the claim language simply requires that the clock generator is "configured to generate a clock signal with which the data processor performs the predetermined processing operation" (i.e., it is not stated that the clock generator provide a clock signal to the host interface). This could be taken to mean any function or component in the circuit on which the data processor relies receives the clock signal. Also, contrary to Applicant's argument, rather than CD-ROM decoder 260 (which comprises of host interface 13) being equivalent to the claimed "data processor", a more correct approach would be that digital signal processor 5 or analog signal processor 4 of Figure 1 to be equivalent to the claimed "data processor". Therefore, since control microcomputer 244 (item 8 of

Figure 1) transmits a command to clock generator 62 regarding whether or not to provide the clock signal to the various components, see Column 8 lines 6-10, it can be seen by the direction in which the control arrows point in Figure 1, that the clock generator 62 does in fact provide a clock signal to the processors 4 and 5. In other words, clock generator 62 would be located between control microcomputer 8 and processors 4 and 5 in Figure 1.

Therefore, the claims stand as previously rejected.

9. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Faisal Zaman whose telephone number is 571-272-

6495. The examiner can normally be reached on Monday thru Friday, 8 am - 5:30 pm, alternate Fridays off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark Rinehart can be reached on 571-272-3632. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

FMZ

Faisal Zaman
Examiner
Technology Center 2100

MARK H. RINEHART
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100